Title: Effects of mask material conductivity on lateral undercut etching in silicon nano-pillar etching

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I. Abstract:

High aspect ratio silicon structures have gained significant interest due to its vast applications. Minimal lateral etch under the mask is essential to achieve very high aspect ratio silicon nanostructures. Previously, we reported that chromium oxide is better than metallic chromium as a hard mask for silicon etching in terms of etch rate and selectivity to resist during mask structure fabriction[1]. Here we report that insulating metal oxide etch mask like chromium oxide also provides less lateral etch than conducting metal etch mask using non-switch "pseudo-Bosch" dry etching.

The mask structure was fabricated by electron beam lithography and liftoff, with all the metal and metal oxide coated by evaporation. Silicon was etched using a non-switching pseudo-Bosch process (Oxford Instrument Plasmalab100, 10 mTorr, 20 W RF power, 1200 W ICP power, 38 sccm C4F8, 22 sccm SF6, 15 ^{o}C, etches Si 390 nm/min)[2]. With etching parameter modification, this non-switching process is also capable of tuning the sidewall taper angle from large positive (cone structure) to large negative etch profile[3,4].

Figure 1 and 2 showed the etched silicon pillar structures. As seen, the amount of lateral etch right underneath the mask is less for Cr_2O_3 and Al_2O_3 mask than Cr or Al masks. For instance, the lateral etching under Cr_2O_3 mask was roughly half that under Cr mask (~7 nm vs. ~14 nm for 1.2 μm etching depth, Figure 1). Figure 3 showed that higher bias power leads to less undercut than lower one, due to increased and more directional physical bombardment by ions. We speculate that, for metal mask, the negative charge taking in from the plasma due to fast electron motion would move to the edge of the mask disk due to Coulomb repulsive force, attracting ions to bombard the area below the mask that results in more lateral etching.

II. Reference:

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III. Image:

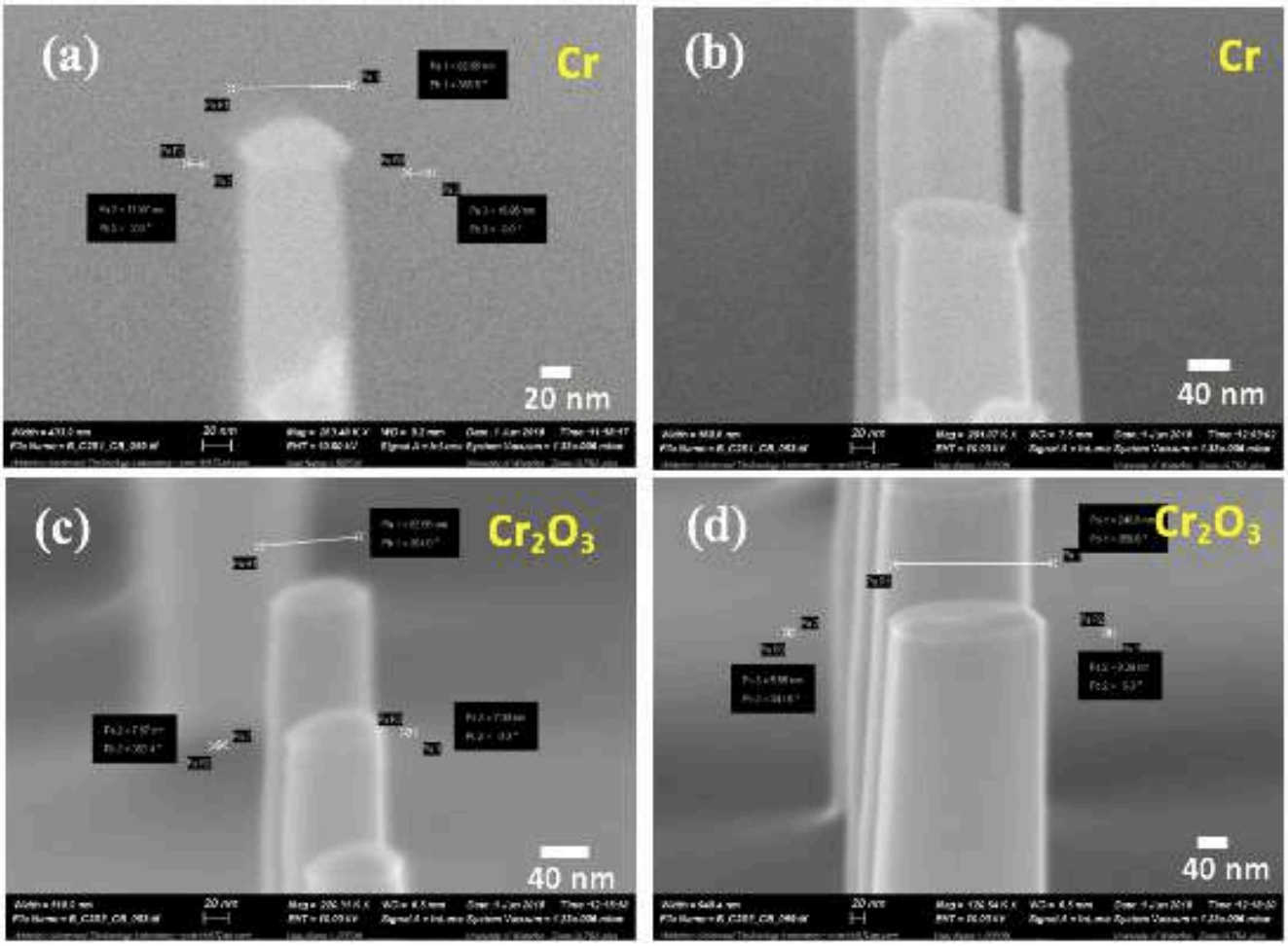


Figure 1. SEM images of pillar structures with etch depth 1.2 um. (a) Cr mask with 100 nm diameter (~14 nm undercut); (b) Cr mask with 200 nm diameter (~13 nm undercut); (c) Cr_2O_3 mask with 100 nm diameter (~7 nm undercut); (d) Cr_2O_3 mask with 200 nm diameter (~7 nm undercut). All are etched using 100 W RF bias power.

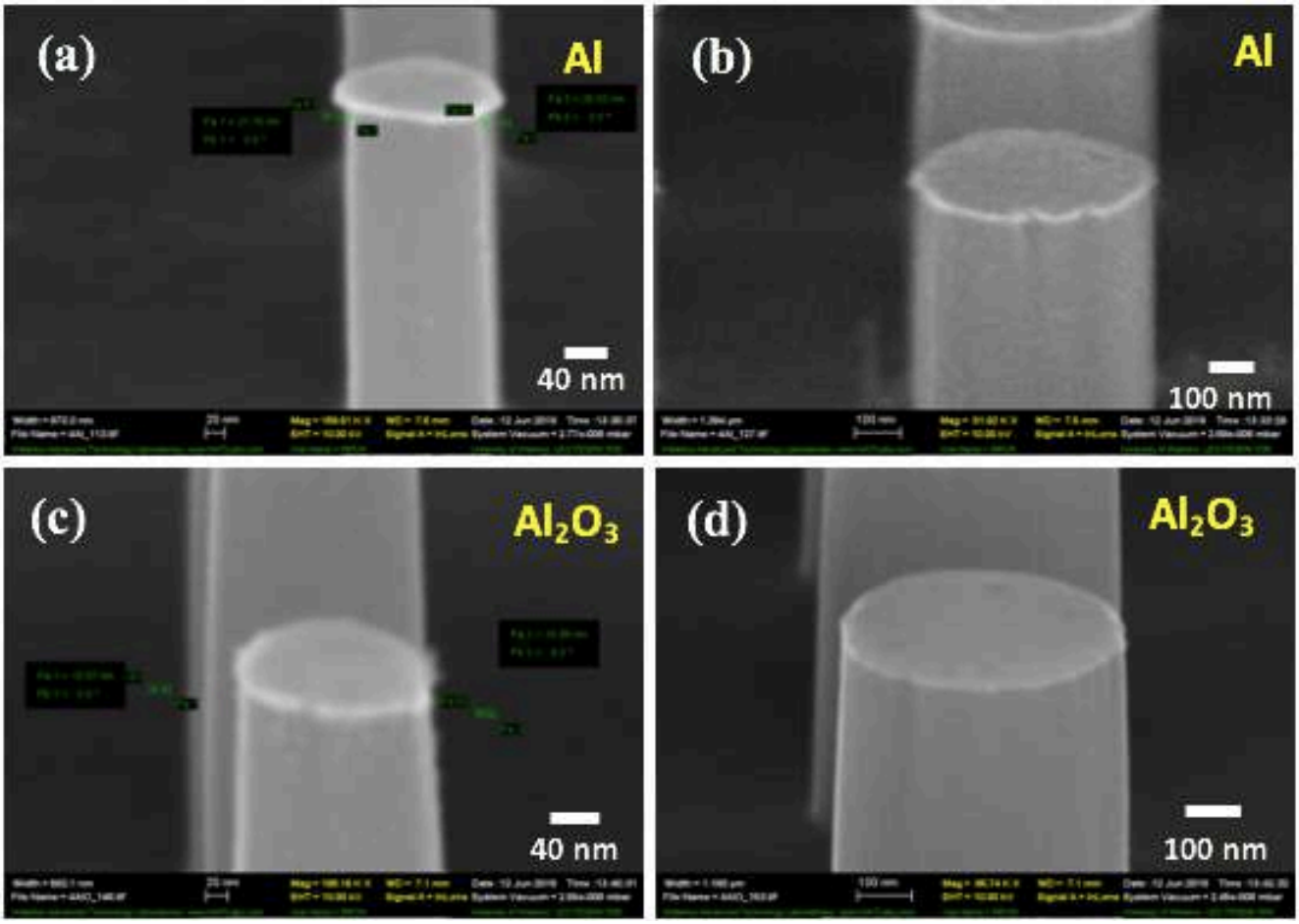


Figure 2. SEM images of pillar structures with etch depth 1.2 um. (a) Al mask with 200 nm diameter (~27 nm undercut); (b) Al mask with 400 nm diameter (~25 nm undercut); (c) Al_2O_3 mask with 200 nm diameter (~12 nm undercut); (d) Al_2O_3 mask with 400 nm diameter (~11 nm undercut). All are etched using 20 W RF bias power.

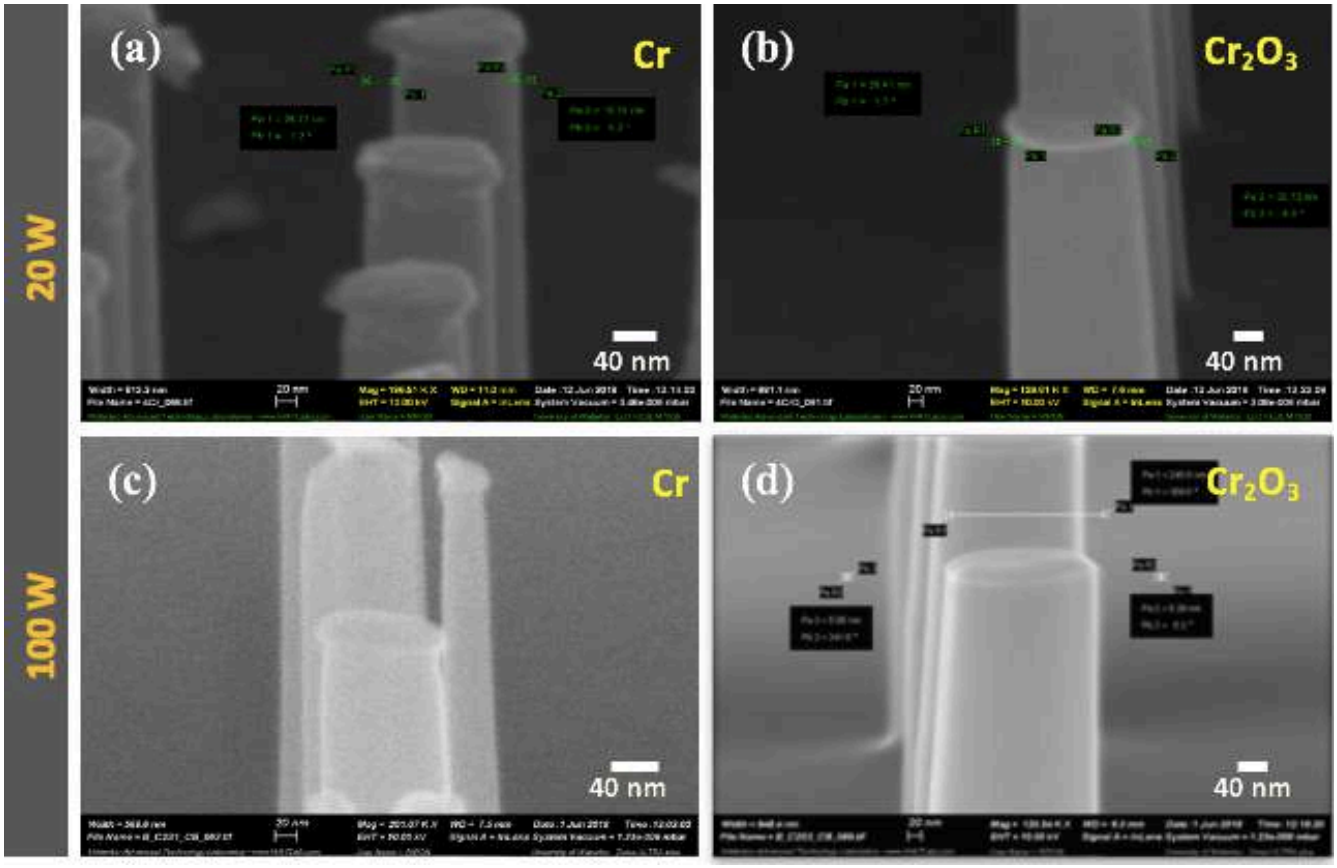


Figure 3. SEM images of pillar structures with etch depth of 1.2 um using various bias powers. (a) Cr mask (~28 nm undercut) with 20 W bias power; (b) Cr_2O_3 mask (~22 nm undercut) with 20 W bias power; (c) Cr mask (~13 nm undercut) with 100 W bias power; (d) Cr_2O_3 mask (~7 nm undercut) with 100 W bias power. The mask diameter of all those pillars was 200 nm.

IV. Biography:

Dr. Ripon Dey has completed his PhD from University of Waterloo in Electrical Engineering and Postdoctoral Studies from School of Engineering, University of Waterloo (UW), Canada. He is the Research Scientist of Waterloo Institute for Nanotechnology (WIN), a premier Nanotechnology Engineering Research Institute in the globe. He has published more than 32 papers in reputed peer reviewed journals including 3 issued patents (Intellectual property) and has been serving as a senior reviewer of Elsevier Engineering. He is also Mitacs Research fellow in UW.

Dr. Dey's research is focused on MEMS/NEMS Engineering, Nano-electronics, Material Engineering, Nano-sensor, nano- and microstructure fabrication.

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