Quilt Packaging® Microchip Interconnect Technology for Biomedical Applications

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Indiana Integrated Circuits LLC

Indiana Integrated Circuits, LLC (IIC)

Formed to commercialize Quilt Packaging (QP) – a ground breaking packaging technology invented at Notre Dame.

- Founded in 2009, based out of South Bend, IN
- Licensing business model (w/prototyping & fabrication support)
- IIC is in-revenue and has experienced steady growth with customers & partners across multiple application spaces (RF/microwave, large format array, power, MEMS, optics, sensors)
- Multiple rounds of investment, currently closing Series A Round
- Si QP process is commercially available at RTI International in NC
- Process development for medium volume requirements is ongoing at Rogue Valley Microdevices in Medford, OR.

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Existing Supply Chain

- RTI International, Inc.
  - ITAR compliant BEOL facility located in Durham/RTP, NC
  - Wafer post-processing for deep etch, plating, CMP, singulation
  - Si & SiC substrates from pieces up to 8” wafers
  - IIC partner since 2012
  - Just started offering QP MPW service June 2015
  - Can support up to 100+ wafer starts per month

- Rogue Valley Microdevices, Inc.
  - Pure-play MEMS foundry located in Medford, OR
  - Wafer post-processing for thin film, etching, litho (deep etch coming)
  - Multiple substrates, up to 8” wafers
  - IIC partner since January 2015 (MIG Tech. Pitch win award)
  - Can support several hundred wafer starts per month

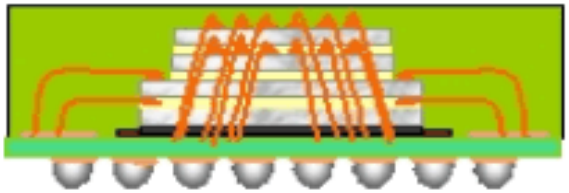
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Why is advanced packaging important for biomedical?

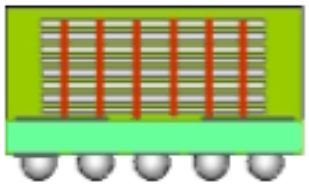
For all of the same reasons advanced packaging has become so important to the industry at large!

- Reduced power consumption (enabling low-power wearable and implantable systems)
- SWAP reduction (system miniaturization for implantable and wearable devices)
- Increased performance (advanced diagnostics, (microfluidics, “Lab On A Chip” approaches, etc.)
- Cost reductions due to reduced part count, wafer yield improvements, IP re-use, etc.

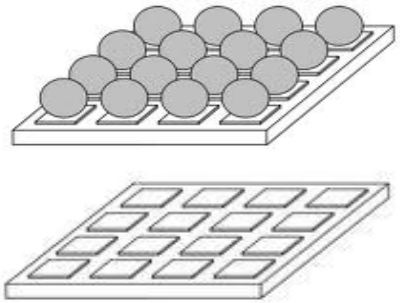
Existing Dense Packaging Approaches: Stacking, TSV, Flip-Chip



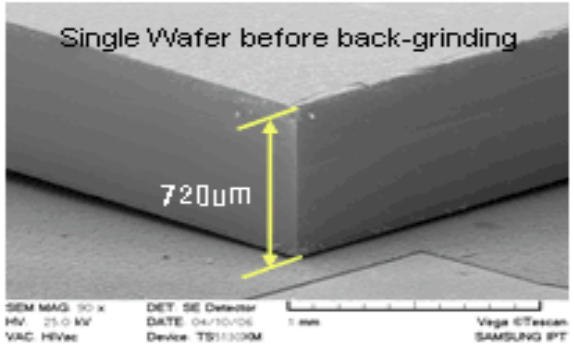
MCP Structure



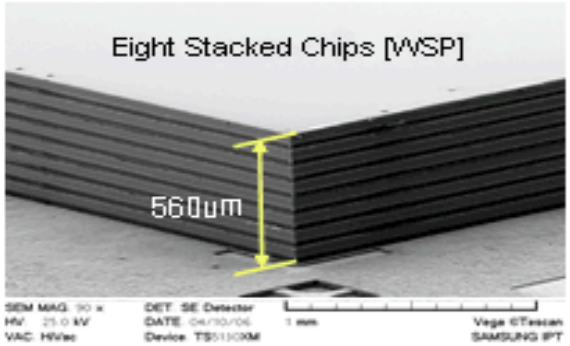
WSP Structure



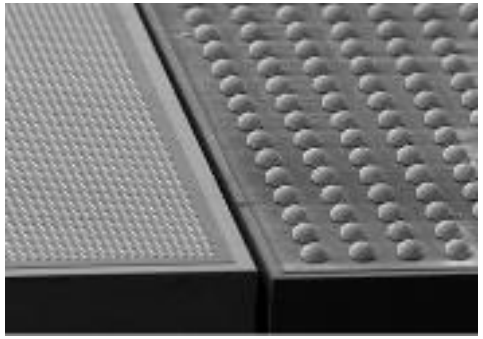
[Thickness Comparison]



Single Wafer before Back-grinding



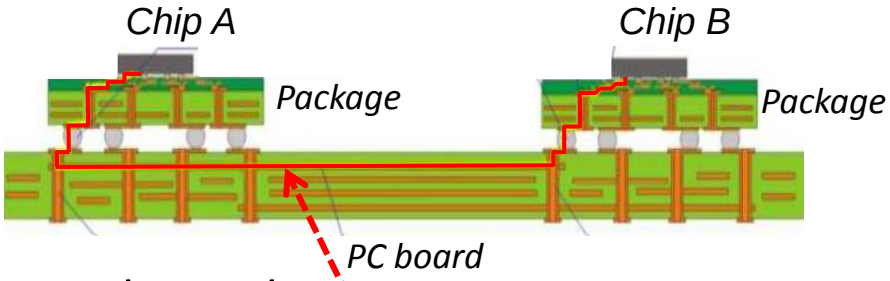
Eight-Chip WSP

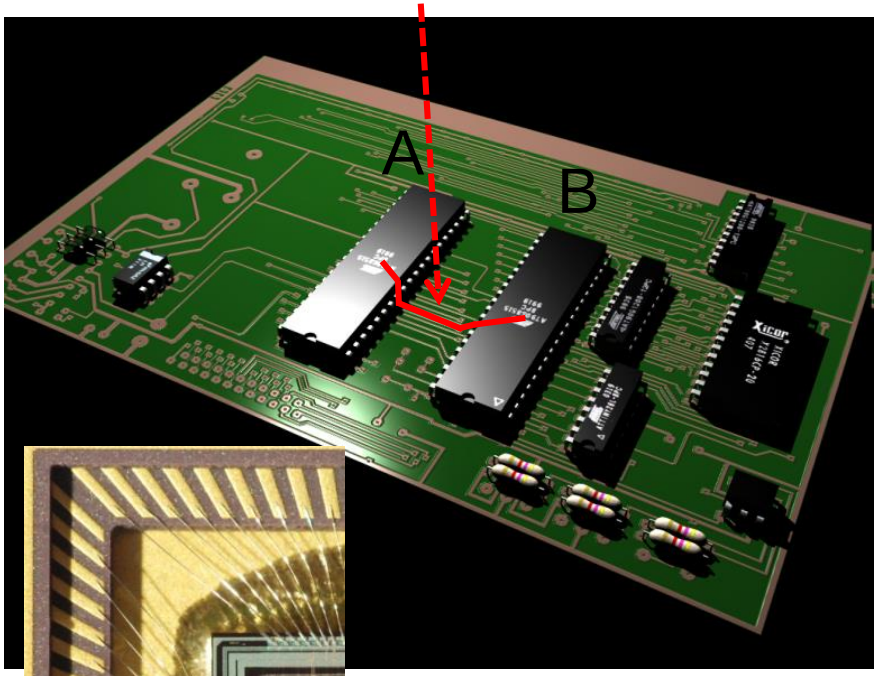


Flip Chip

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The Problem:
Existing Microchip Packaging

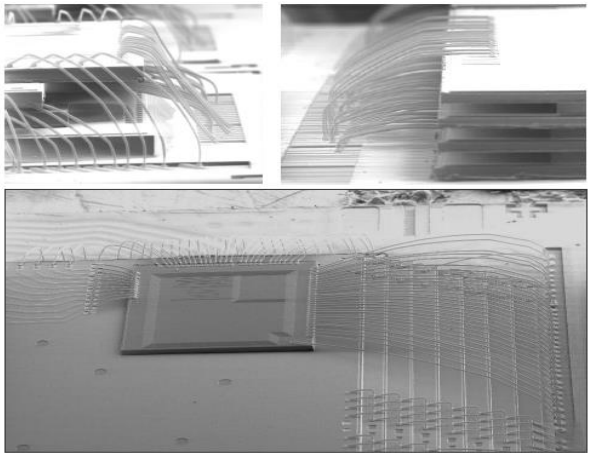




"…Overall performance, cost, size and functionality of a system will be limited by….the off-chip interconnects."

-International Technology Roadmap For Semiconductors

Existing technologies waste:

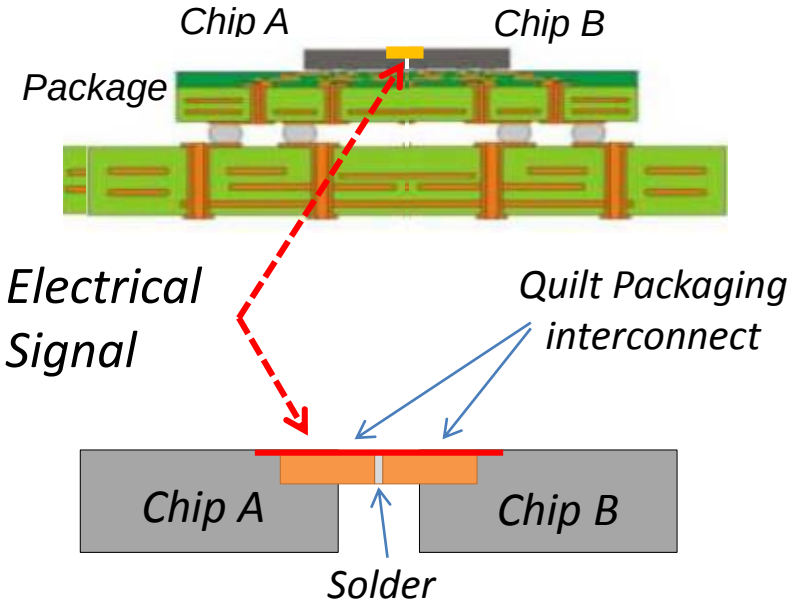


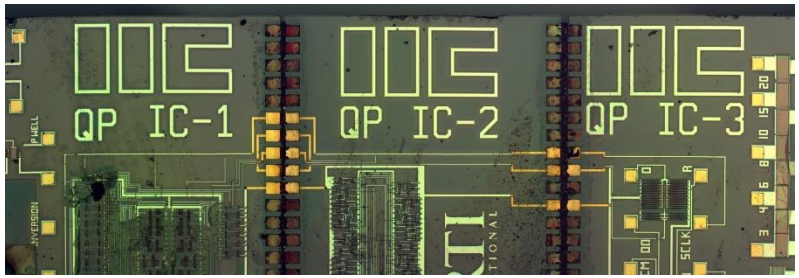
- Power
- Time
- Money
- Space

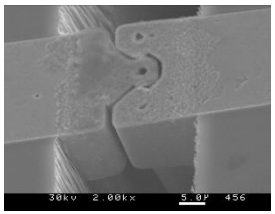
Now a system constraint!

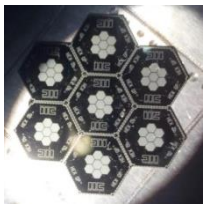
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The Solution:
Quilt Packaging Interconnect Technology









Quilt Packaged chipsets and interconnects

Quilt Packaging is a patented, *direct* edge-to-edge chip interconnect technology that can be implemented in disparate materials and technologies.

Quilt Packaging enables 10x to 100X improvement!

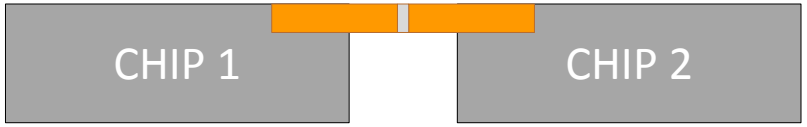
- Power--- 10x lower parasitic losses
- Time---10x faster
- Money---Order of magnitude total system cost savings
- Space---Dramatic form factor reduction

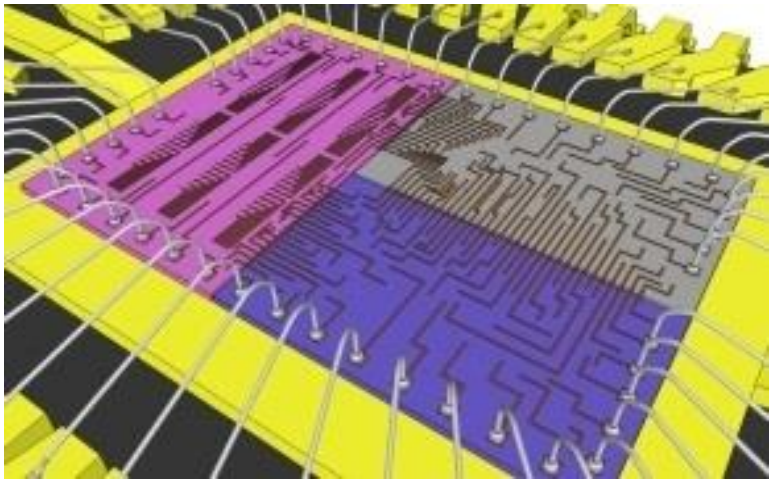
Quilt Packaging enables new system designs

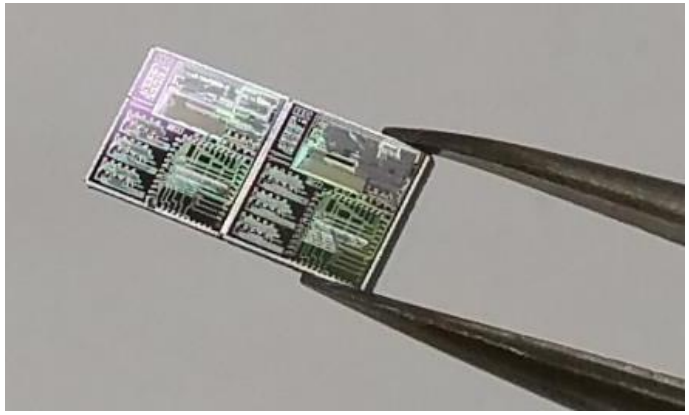
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Quilt Packaging (QP) Technology

- Edge-connections joined to create multi-chip “quilt,” developed at Notre Dame
- “Monolithic” assemblies from same or disparate materials & process technologies
- Extremely low impedances
- Enables optimization for cost and functionality
- Industry-standard tools and fabrication processes (available in Si at RTI)



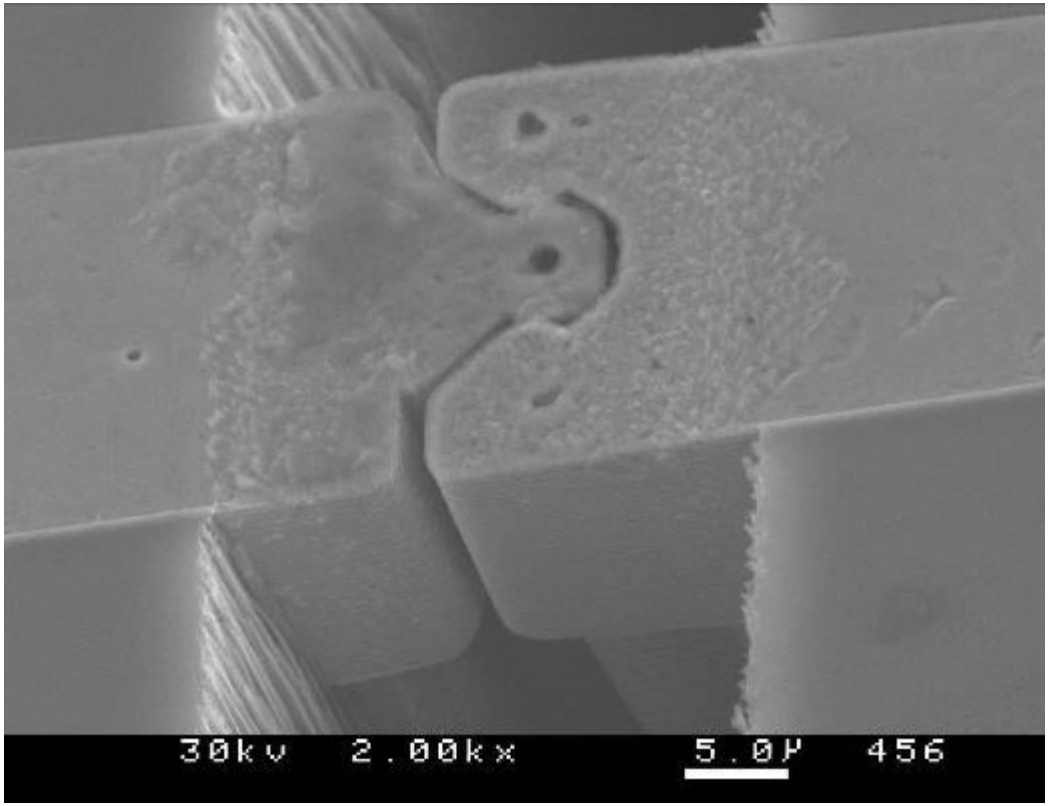




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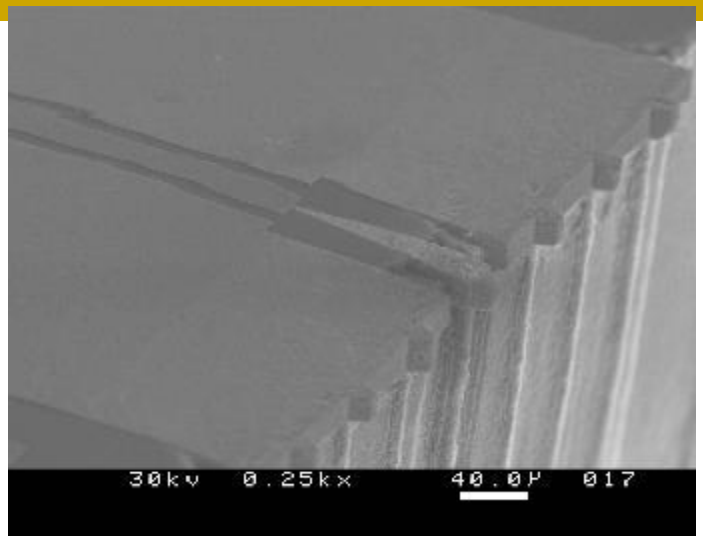
QP-Interconnect Structures

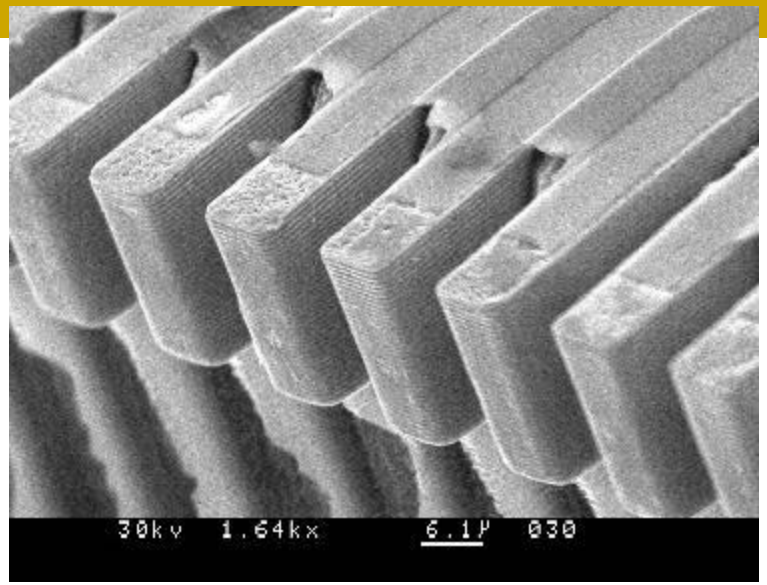
- Edge connection structures called “nodules”
- Solid metal, typically 5-500 um wide, ~ 20-50 um thick
- Customizable shapes-including interlocking-*enables sub-micron chip alignment*

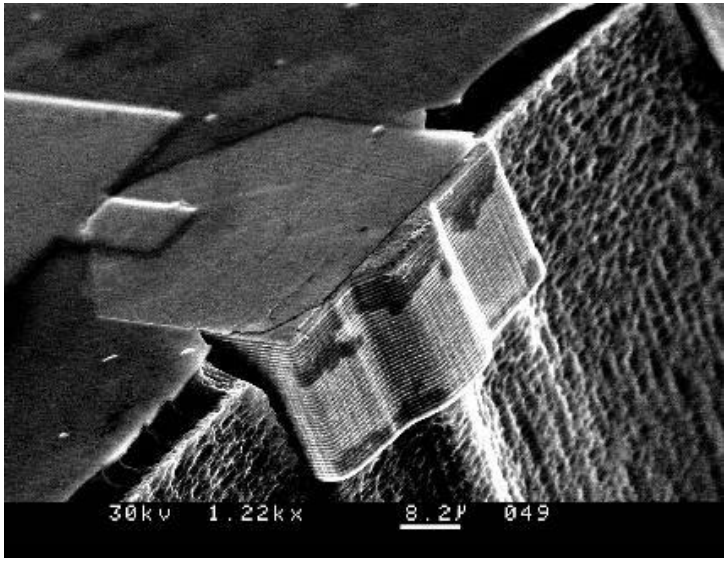


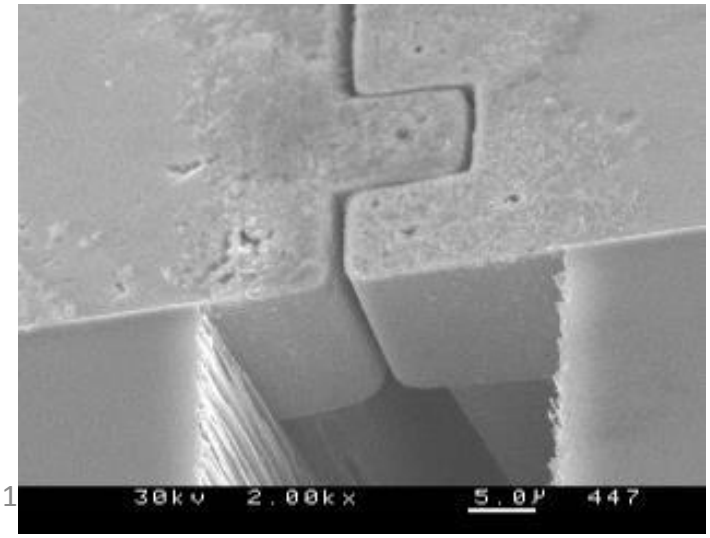
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QP Customizable I/O



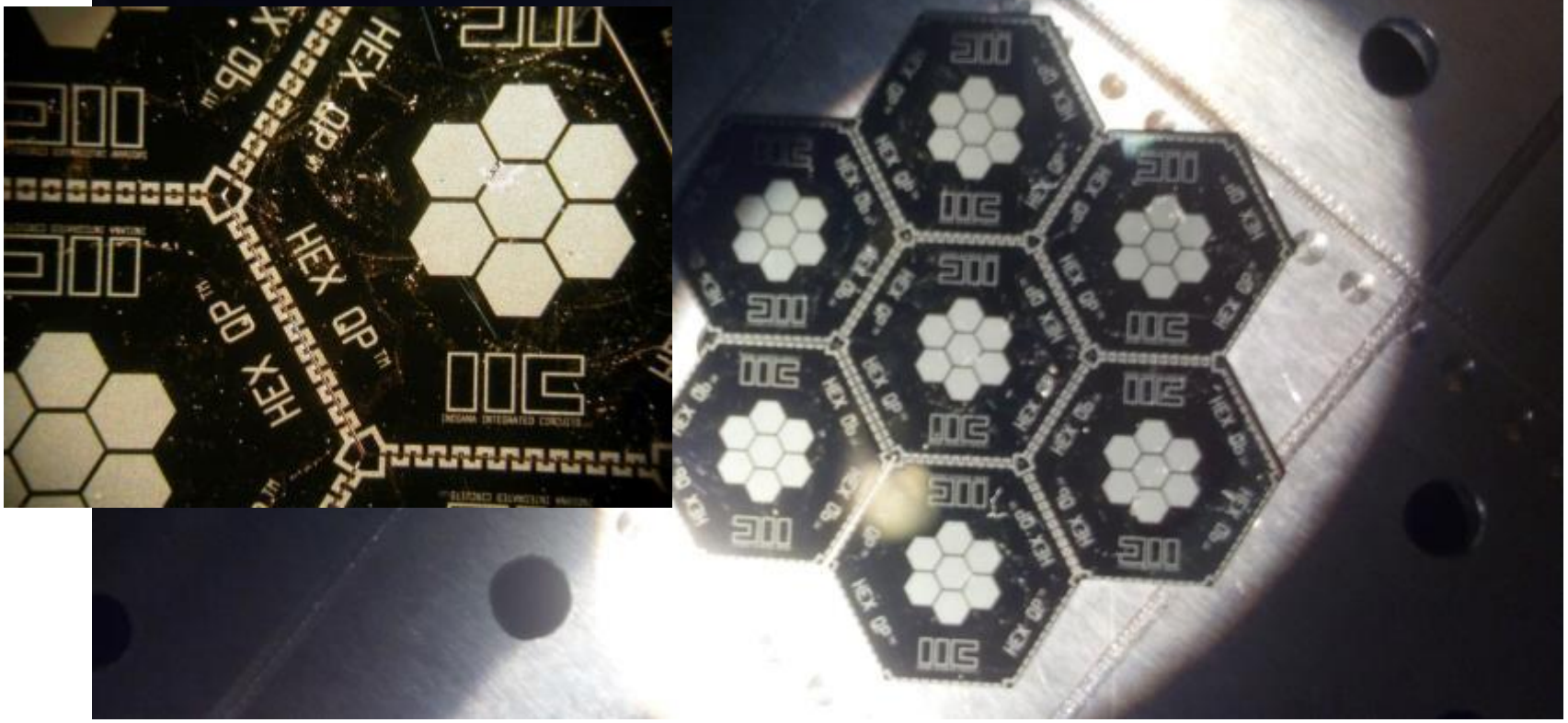






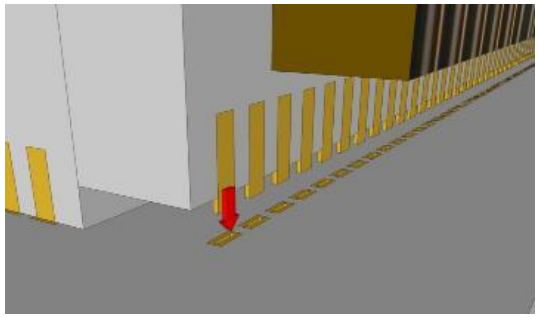
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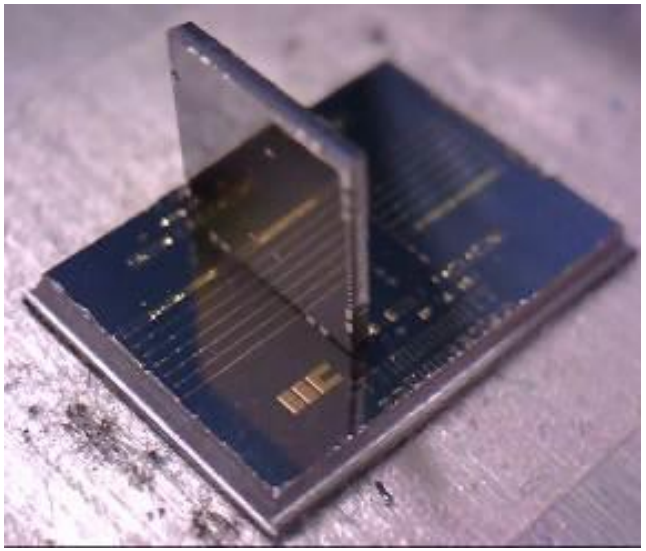
QP Supports Customized Geometries example - HexQP™

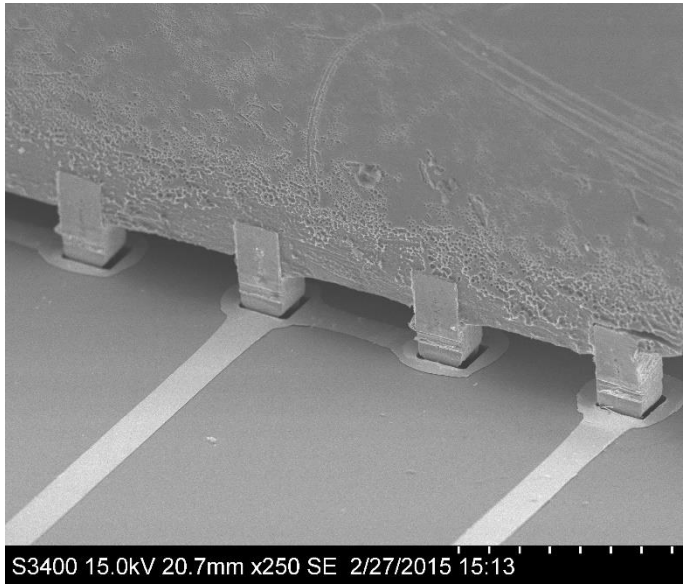


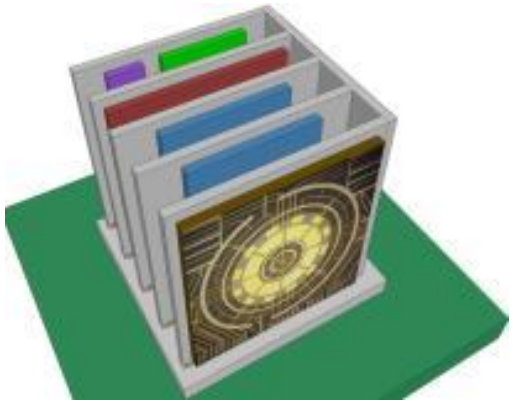
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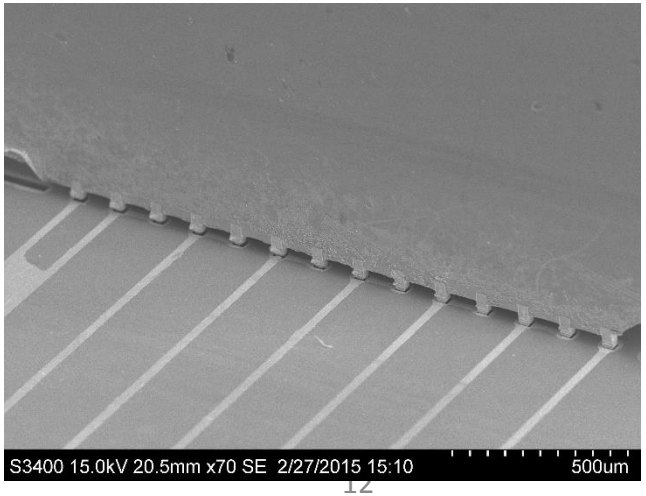
“3DQP” Variations

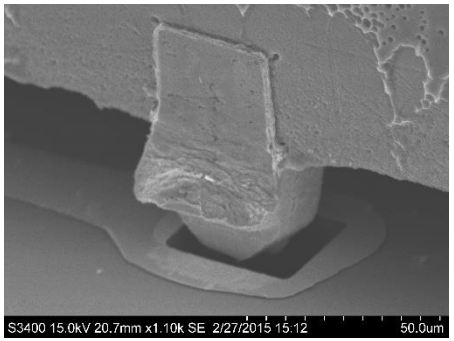


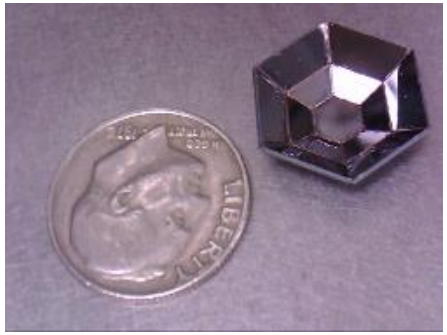






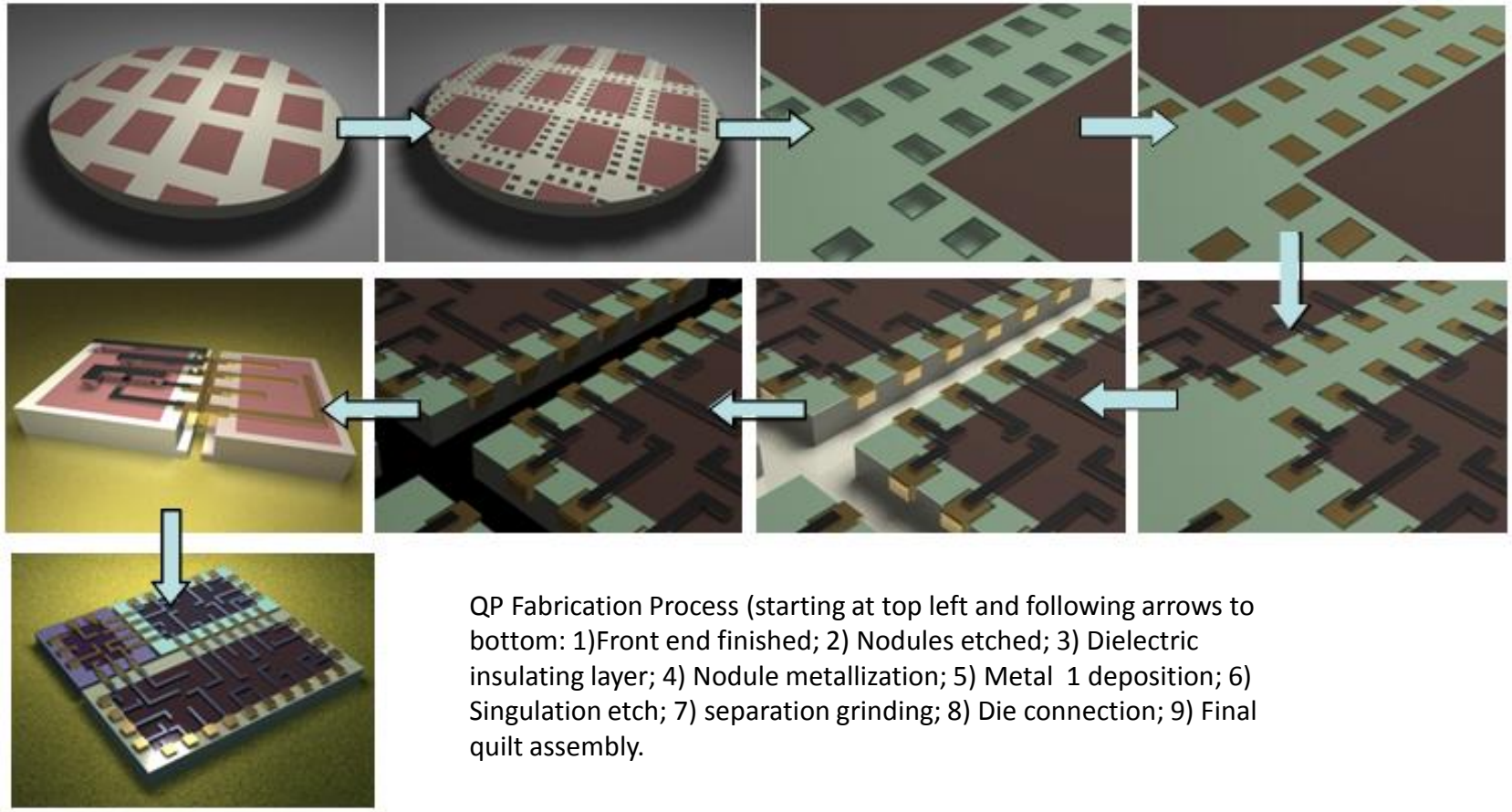






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Quilt Packaging Fabrication Process



QP Fabrication Process (starting at top left and following arrows to bottom: 1)Front end finished; 2) Nodules etched; 3) Dielectric insulating layer; 4) Nodule metallization; 5) Metal 1 deposition; 6) Singulation etch; 7) separation grinding; 8) Die connection; 9) Final quilt assembly.

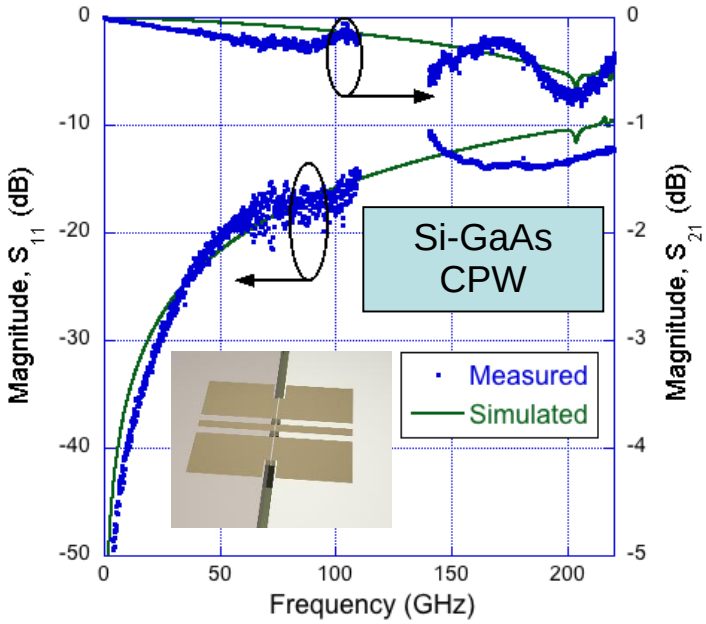
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Why use Quilt Packaging?

- Optimized integration of disparate materials and process technologies (Si, SiGe, AlN, GaAs, SiC, GaN, more)
- Chip partitioning for optimal yield/functionality
- Extremely low-loss, dense interconnect technology
- Sub-micron chip-to-chip alignment (Optical, Microfluidics)
- System miniaturization, new architectures
- Reduced power dissipation, die size, design cycle time
- Variety of interconnect geometries & sizes available simultaneously
- Increased IP flexibility, security & design re-use
- Complementary with existing packaging approaches---can be combined w/TSV, WB, bumping, etc.

Quilt Packaging: Electrical Performance

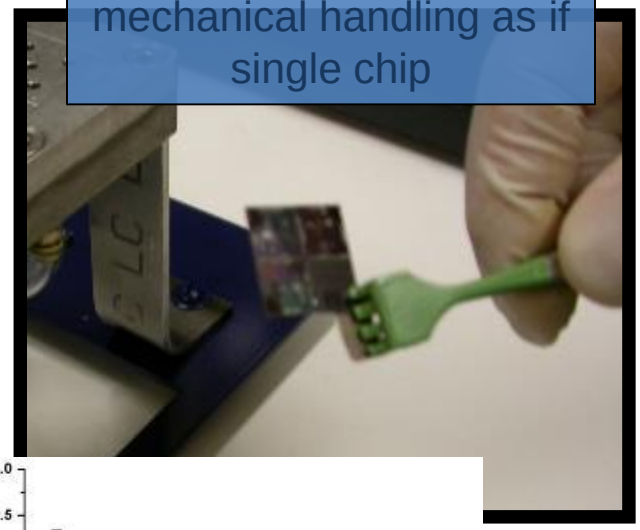
- Homogeneous (e.g. Si-Si, GaAs-GaAs) and heterogeneous (Si-GaAs, Si-InP) interconnects demonstrated
- Excellent RF/millimeter-wave, high-speed digital performance:
  - $S_{21} \leq 0.75$ dB to 220 GHz
  - 43 Gb/s eyes with no impairment
- Power applications:
  > 10 A through 30 µm x 20 µm nodules without damage (power modules with ultra-low parasitics & increased power density)
- Extremely low loss, dense I/O

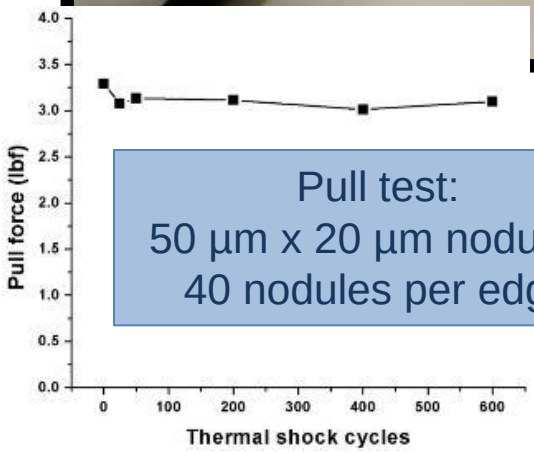


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Quilt Packaging: Mechanical Performance

- Interconnects are mechanically **robust**
- Interconnected modules can be handled like **larger chip** (e.g. pick & place, etc.)
- Preliminary **pull testing** requires large force before failure; resistant to thermal shock,
- Preliminary thermal cycle, shock, cryo testing shows no show-stoppers



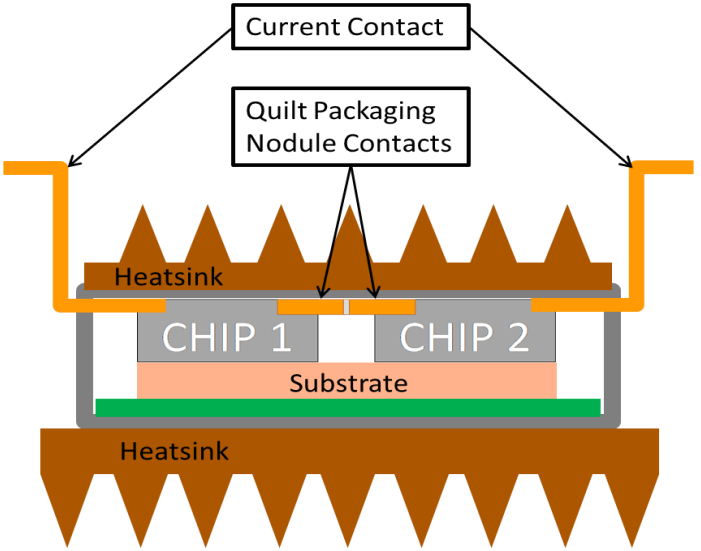


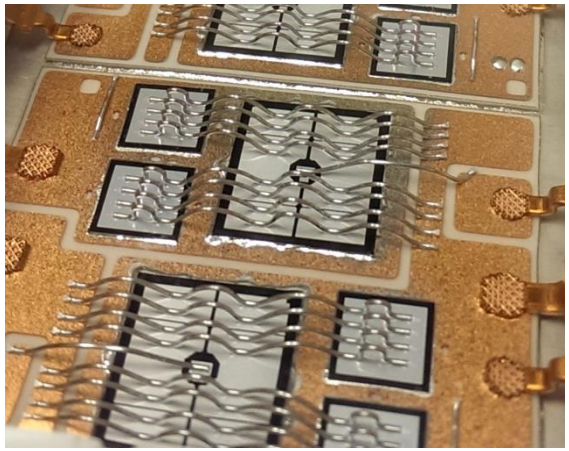
Pull test:
50 µm x 20 µm nodules,
40 nodules per edge

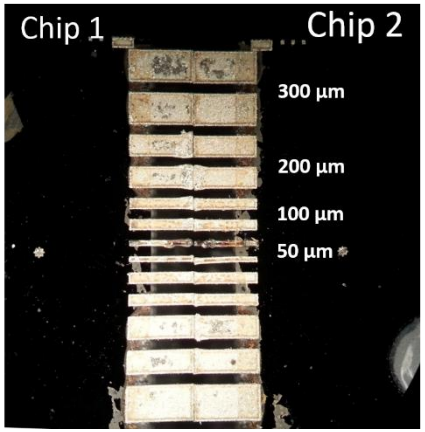
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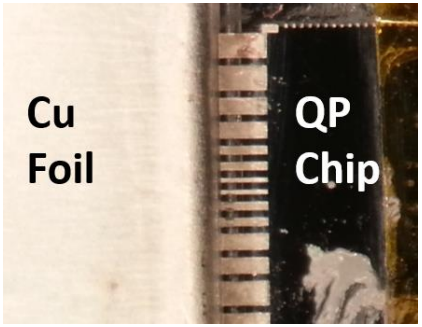
Application Example: Power Supplies

- Dramatic reduction in parasitics (chip-chip and module)
- Faster switching/improved transient control
- Increased power density
- Reduced BOM & form factor





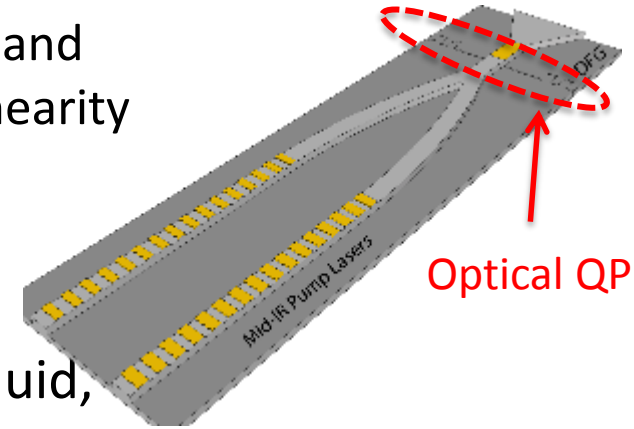


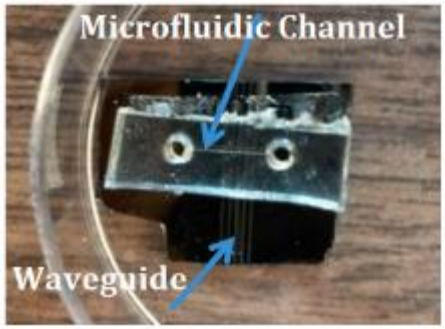


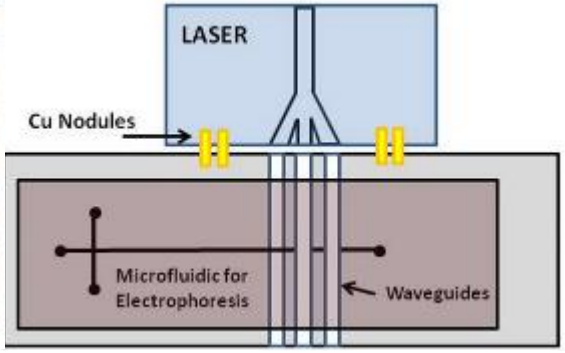
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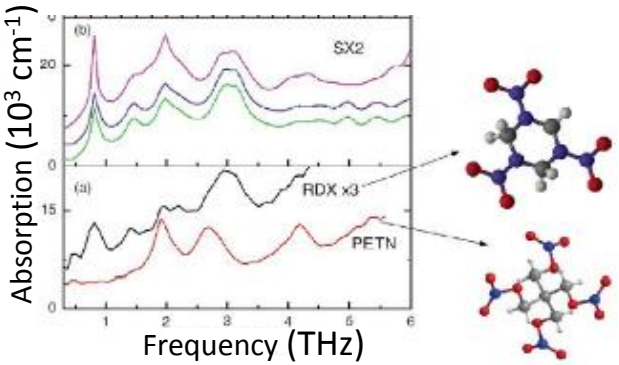
Applications Space: Optoelectronic Sources & Sensors

- Tunable, high-power THz sources
  - Independently optimize mid-IR pump lasers and difference frequency generator (DFG) nonlinearity
  - High power (~mW), room-temperature, CW
- Sensitive and specific stand-off material detection
- Integration with microfluidics for on-chip liquid, gas analysis and sensing









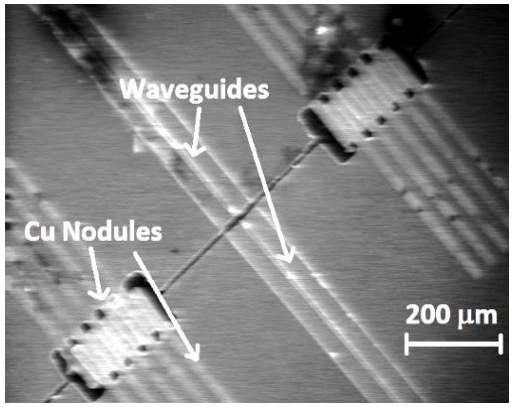
A.G. Davies *et al., Materials Today* **11**, 18 (2008).

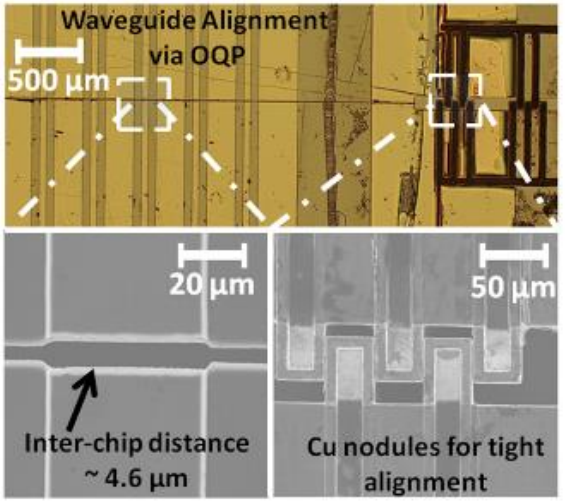
(Courtesy S. Howard & S. Hoffman, Notre Dame)

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Application Space: Optoelectronics and Photonics

- Precision integration:
  - High-density, low-loss silica planar optical waveguides
  - High-performance III-V emitters & detectors
- Sub-wavelength passive chip-to-chip alignment
- Experimentally demonstrated:
  - Lateral alignment: << 1 µm
  - Axial positional tolerance: < 5 µm
  - Insertion loss ≤ 2 dB in mid-IR



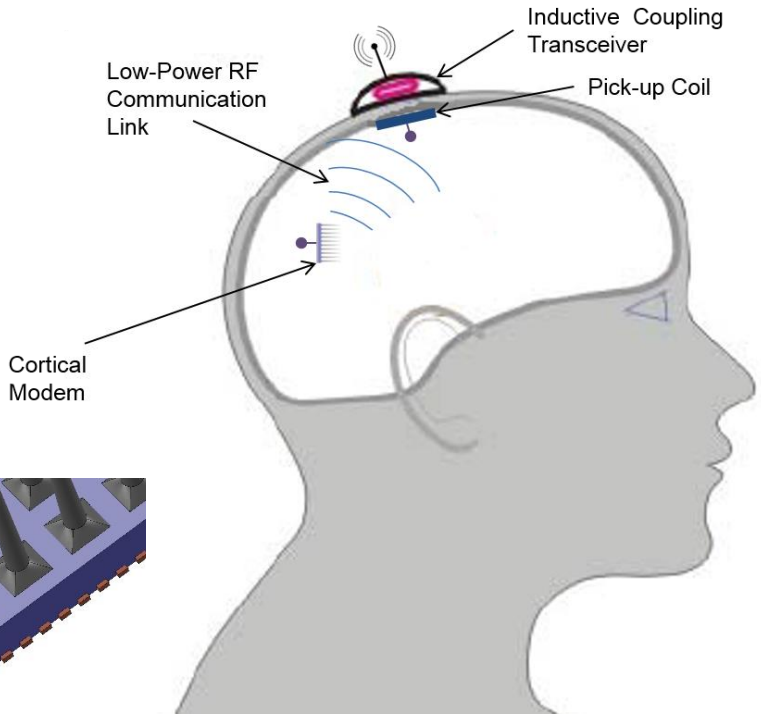


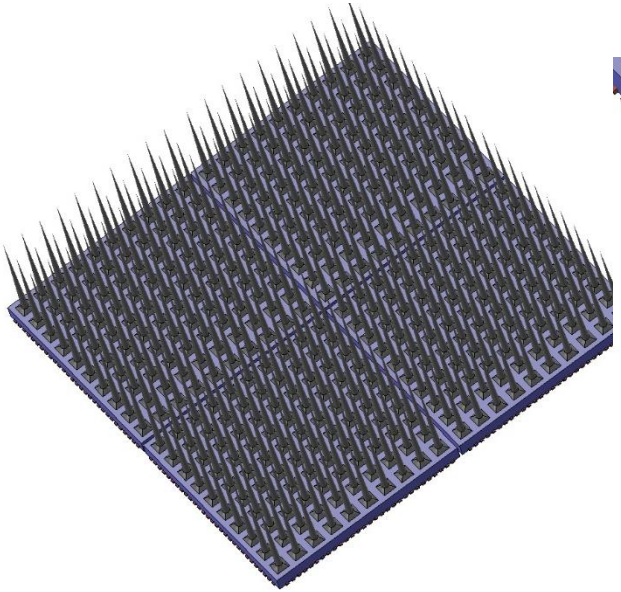
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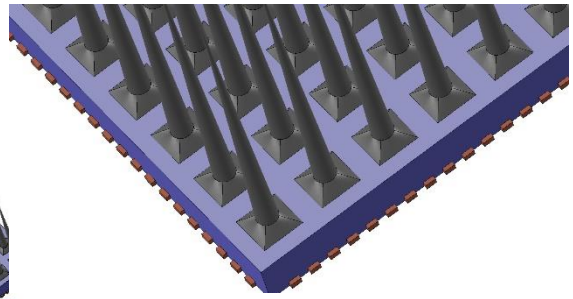
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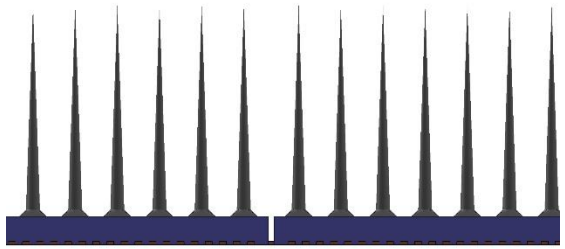
Application Example: System Miniaturization for Implantables

- Extremely low-loss interconnect (low power)
- Decreased form factor
- Modularity (design & yield)







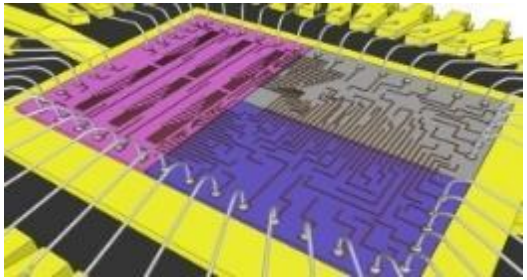


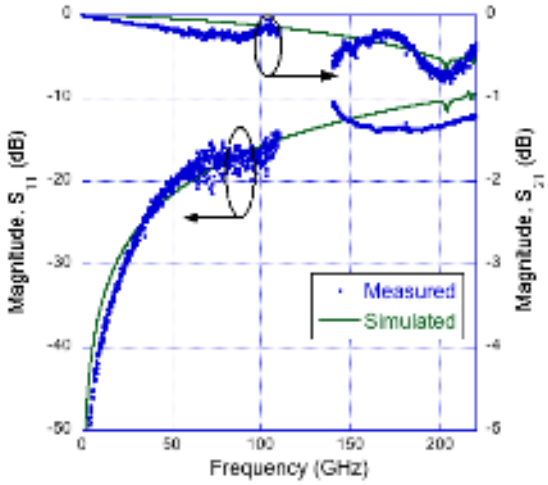
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Summary / Conclusions

- Quilt packaging features:
  - Ultra-wide electronic bandwidth: insertion loss ≤ 0.75 dB to 220 GHz
  - Heterogeneous integration across materials and process flows
    - Si, III-V, SiC, GaN, silica optical waveguide, microfluidics---Best device/material/process for each function
  - System miniaturization & new system architectures/designs





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